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Abstract. This paper presents a study on an integrated technology: Fully-Depleted-Silicon-On-Insulator (FDSOI) at a 28nm node. FDSOI results are compared to another technology: Complementary-Metal-Oxide-Semiconductor (CMOS) 350nm. The aim of this work was to demonstrate the advantages of using FDSOI technology in RF energy scavenging applications. Characteristics of transistors are pointed out and results showed an improved 22%-output voltage gain for a series rectifier and a 13%-output voltage gain for a Dickson charge pump in FDSOI technology compared to CMOS, for an input voltage and power of 0.5 V and 0 dBm respectively. Those results allowed to prove that FDSOI 28nm is a better technology choice for energy scavenging and low-power applications.

1. Introduction

Nowadays, microelectronic field aims to focus more and more on systems miniaturization as the reduction of power consumption without compromises on the required performances. Based on these objectives, some studies have been realized on energy conversion applications in [1], [2] and [3]. In addition to that, energy scavenging applications are considered to reduce the power consumption as in [4]. Moreover, reducing size could make evolve circuits like shown in [5]. RF energy scavenging is also present at nanoelectronic scale, which is designed to power integrated low-energy devices and sensors. The primary features and challenges of the FDSOI compared to CMOS has been described in literature as in [6]. Based on these facts, the aim of this study was to compare two technologies and to point out the advantage to use the emergent technology FDSOI in integrated applications such as RF-DC and DC-DC (charge pump) conversions applied to energy scavenging and low-power. This paper offers comparison simulations between CMOS 350nm and FDSOI 28nm technologies. Section 2 describes the remarkable transistors parameters. Then, the obtained output voltages of an RF rectifier and a Dickson charge pump structure [7] are discussed in section 3 and 4. Simulations were realized with Cadence Software by considering raw components. The ultimate goal of this study was to demonstrate that FDSOI 28nm is a suitable technology for RF energy scavenging.

2. Transistors characteristics

2.1. Transistors threshold voltages

This subsection presents studies of the drain current curves of different transistors of the technologies. FDSOI 28nm offers two interesting N-channel transistors: LVT (Low Voltage Threshold) and RVT (Regular Voltage Threshold). For CMOS technology, this work focuses on the

N-channel NMOS only. The following simulation gave the voltage threshold of the transistors by plotting the drain current Id for a drain voltage (Vds) of 1V and a gate voltage (Vgs) that varies from -1 V to +3 V. Results showed a voltage threshold of 200 mV for the LVT and 400 mV for the RVT in FDSOI 28nm. The same simulation was done for the NMOS transistor in CMOS 350nm. A threshold of 600 mV was found for the NMOS. These results show the best possible performances in FDSOI for low-power applications. Table 1 shows the threshold values.

	FDSOI LVT	FDSOI RVT	CMOS NMOS
Threshold Voltage	200 mV	400 mV	600 mV

Table 1. Threshold values of the studied transistors

2.2. Diode-connected transistor substrate connexion

This subsection presents a better way to connect the substrate connection of a four-connections transistor in diode-connected mode. The four-possible connexions are Gate, Drain, Source and Substrate. According to schematic on figure 2 and results on figure 1, the rectifying process performed better when substrate was connected to gate and drain. The advantages were therefore a good rectification with less current in negative part and a higher voltage. Figure 1 shows limits of the substrate connexion.

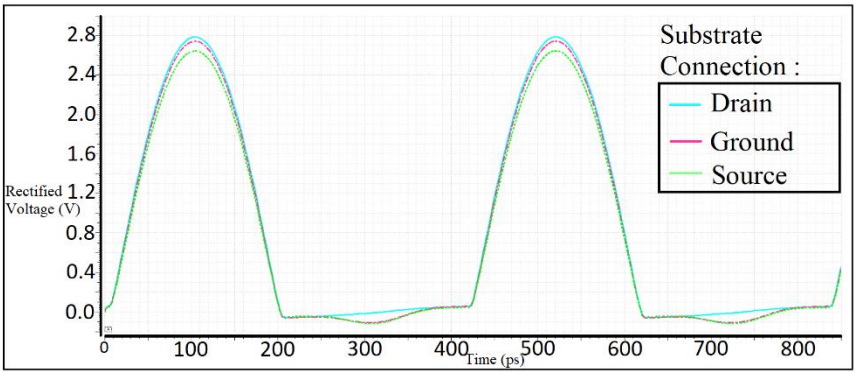

Figure 1. Transistors substrate connexion effect on rectified voltage

3. Rectifier

This section presents a comparison between simulated results obtained with a simple RF-DC rectifier, where the diode was replaced by LVT, RVT or NMOS transistors in diode-connected mode. Figure 2 shows the corresponding schematic.

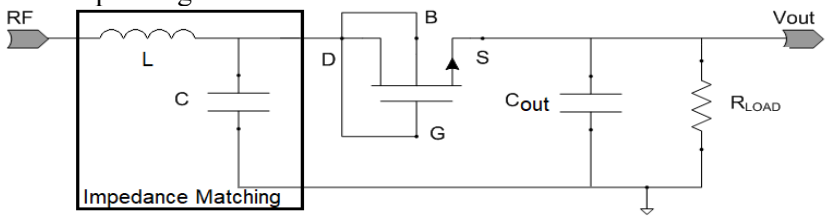

Figure 2. Schematic of a diode-series rectifier

The input power was set to 0 dBm at a frequency of 2.4 GHz. The output capacitance was set to 160 pF and the load resistance to 1 GΩ in order to show the best output voltages in this case. Figure 3a shows the output responses of the rectifier without using the impedance matching.

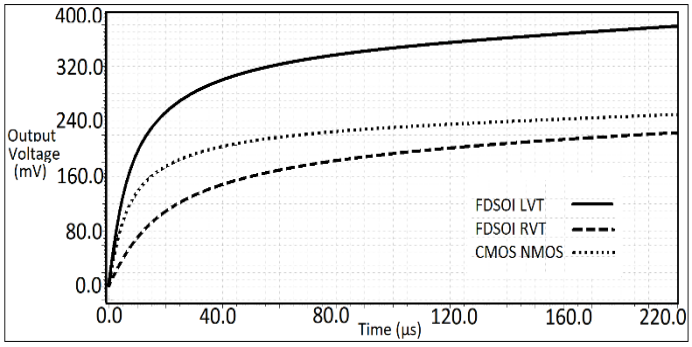

Figure 3a. Output voltages of rectifier

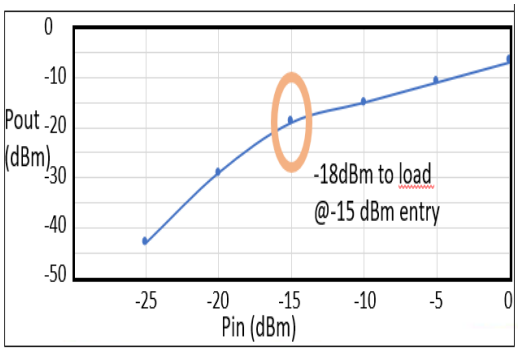

Figure 3b. Output power of an impedance matched rectifier

As shown on figure 3a, the use of a FDSOI LVT transistor allowed a simple rectifier to produce 390 mV output while the output voltage reaches only 240 mV in CMOS technology. The performance gain was therefore 22% on an RF simulated output voltage in favour of FDSOI technology. These performances came from the fact that FDSOI LVT threshold is lower than CMOS and this last parameter is linked to the rectifying diode-mode connection. The RVT transistor is not better than the NMOS in this case because it's default channel length is 4 times bigger than LVT. Channel length is a critical parameter in energy scavenging, more than channel width. Figure 3b shows the output power of a matched L-C rectifier for an input power that goes from -25 dBm to 0 dBm. The matching network allowed a maximum power transfer between the input generator and the transistor. A decent efficiency of 52% at -15 dBm was reached.

4. Charge Pump

This section presents a comparison between simulated results obtained with a classic 4-stages Dickson charge pump shown in [7] where the diode-connected transistors are replaced by LVT, RVT or NMOS. The input voltage was set to 0.5 V, the clock Vpp was 1V with a frequency of 100 KHz and the output resistance was 100 MΩ. Figure 4a shows the charge pump schematic and figure 4b shows the output responses of the charge pump.

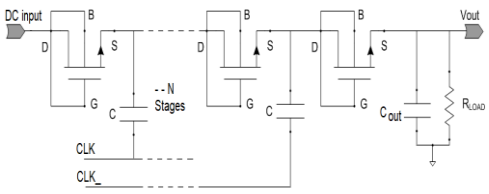

Figure 4a. Charge pump schematic

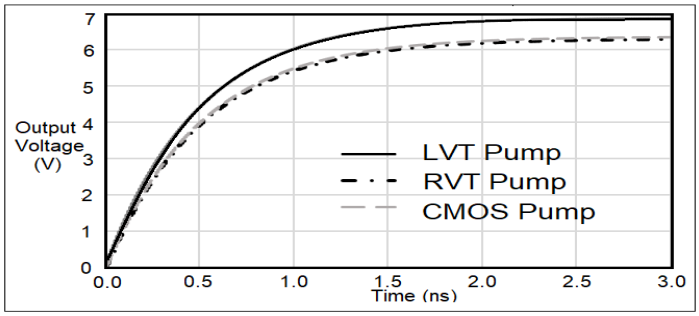

Figure 4b. Output voltages of charge pump using different transistors

As shown in figure 4b, the charge pump that operates with LVT diode-connected transistors achieved better performances than RVT and NMOS responses. The output voltage was 7 V for LVT charge pump while it was higher than 6 V for RVT and CMOS. In this case, a nearly 13%-output voltage improvement was scored by LVT response compared to CMOS because of its low voltage. In addition, it is important to mention that default dimensions of LVT are smaller than NMOS, typically a hundred nano-meters compared to a dozen of micro-meters.

To go further, a 4-stages Dickson circuit was simulated using optimal parametric values with FDSOI LVT. The pump performed up to 3V-output voltage from a 250mV-input with no load. An optimized circuit gave an output of 600 mV at 160 µA. Table 2 compares this work to literature.

Work	**[1] Moisiadis 2000**	**[2] Bhalerao 2007**	**[3] Chen 2010**	**This work**	
Type of work	Simulation	Simulation	1-Chip Integration	Simulation	
Process	Standard CMOS	Standard CMOS	65nm CMOS	28nm FDSOI	
Number of stages	4	4	3	4-Dickson based	
Input-Voltage	1.2 V	1.5 V	0.18 V	0.25	1.5 V
Output Voltage	3.5 V	6 V	0.5 V	0.6	11.4 V
Gain	2.9	4	2.78	2.4	9.5
Load	~58 kΩ	~133 kΩ	50 kΩ	3750 Ω	133 kΩ
Output-Power	~210 µW	~270 µW	5 µW	96 µW	969 µW

Table 2. Work comparison

Conclusion

This paper presents a study on two integrated technologies for RF energy scavenging. FDSOI 28nm and CMOS 350nm performances was compared. The FDSOI LVT transistor was particularly pointed out for its best voltage threshold and characteristics that allow higher output voltages over CMOS in low-voltage RF-DC and DC-DC conversions while reducing the overall dimensions. FDSOI technology is more expensive than CMOS but offers many advantages as a smaller die size and better performances. These comparison results lead to the choice of FDSOI technology for the design of a complete integrated rectifying module for RF energy scavenging.

Acknowledgement

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