Rectenna Design for RF Energy Harvesting using CMOS 350nm and FDSOI 28nm

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***Abstract*—The need for the reduction of energy consumption and size of microelectronic circuits is increasingly in demand. To support this request, this paper presents a comparison study on two integrated technologies: FDSOI 28nm and CMOS 350nm. The aim of this work was to compare the performance of these two technologies for the design of a rectifier and a Dickson charge pump for rectenna application. The results showed an improved 22%-output voltage gain for a given simple rectifier and a 16%-output voltage gain for a Dickson charge pump in FDSOI technology compared to CMOS, for an input voltage and power as low as 0.5 V and 0 dBm. Those results allowed to prove that FDSOI 28nm is a better technology choice for Energy Harvesting and Low-Power applications.**

I. INTRODUCTION

Nowadays, microelectronic field aims to focus more and more on systems miniaturization as the reduction of power consumption without compromises on the required performances. With these objectives, some studies have been realized on energy conversion applications in [1], [2] and [3]. In addition to that, energy harvesting applications are considered to reduce the power consumption as in [4]. And, reducing size could make evolve circuits like shown in [5]. RF energy harvesting is also present in nanoelectronic scale, which is designed to power integrated Low-Energy devices and sensors. The primary features and challenges of the FDSOI compared to CMOS has been described in literature as in [6]. On these facts, the aim of this study was to compare two technologies and to point out the advantage to use the emergent technology FDSOI in integrated applications such as RF-DC and DC-DC (charge pump) conversion applied to energy harvesting and Low-Power. Fig. 1 shows the schematic of a simple RF-DC rectifier.

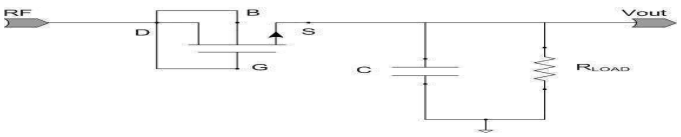

Fig. 1. Schematic of the RF/DC rectifier

This paper offers comparison simulations between the CMOS 350nm and the FDSOI 28nm technologies on the remarkable transistors parameters in section 2. Then, the obtained outputs voltages of an RF rectifier and a Dickson charge pump structure [7] are discussed in section 3 and 4. The simulations was realized with Cadence Software by taking in account raw components. The ultimate goal of this study was to choose which technology is the best for the design of an integrated rectenna.

II. TRANSISTORS PARAMETERS

This section presents the studies of the drain current curves of the different transistors of the technologies. FDSOI 28nm offers two interesting N-channel transistors: LVT (Low Voltage Threshold) and RVT (Regular Voltage Threshold). For CMOS technology, this work focuses on the N-channel NMOS only. The following simulation gave the voltage threshold of the transistors by plotting the drain current Id for a drain voltage (Vds) of 1V and a gate voltage (Vgs) that varies from -1 V to +3 V. Results showed a voltage threshold of 200 mV for the LVT and 400 mV for the RVT in FDSOI 28nm as shown in Fig. 2.

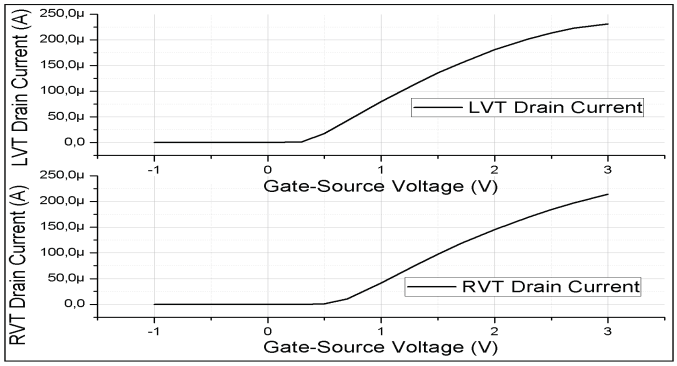

Fig. 2. Simulated parameters Id (Vgs)

The same simulation was done for the NMOS transistor in CMOS 350nm. A threshold of 600 mV was found for the NMOS. These results showed the best possible performances in FDSOI for Low-Power applications.

III. RECTIFIER OUTPUT VOLTAGE RESPONSE COMPARISON IN CMOS AND FDSOI

This section presents a comparison between simulated results obtained with a simple RF-DC rectifier, where the diode was replaced by LVT or NMOS in diode-connected mode as shown on Fig. 1. The input power was set to 0 dBm at a frequency of 2.4 GHz. The load capacitance was set to 160 pF and the load resistance to 1 GΩ. The output responses of the rectifier are shown in Fig. 3.

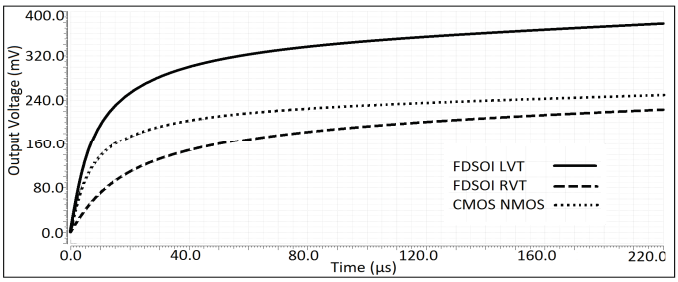

Fig. 3. Output voltage of the RF Rectifier for LVT and NMOS transistors.

As shown in Fig. 2, the use of a FDSOI LVT transistor allowed a simple rectifier to produce 390 mV output while the output voltage reaches only 240 mV in CMOS technology. The performance gain was therefore 22% on an RF simulated output voltage in favor of FDSOI technology.

IV. CHARGE PUMP OUTPUT RESPONSE COMPARISON IN CMOS AND FDSOI

This section presents a comparison between simulated results obtained with a classic 4-stages Dickson charge pump shown in [7] where the diode-connected transistors are replaced by LVT, RVT or NMOS. The input voltage was set to 0.5 V, the clock Vpp was 1V with a frequency of 100 KHz and the output resistance was 100 MΩ. The output responses of the charge pump are shown in Fig. 4.

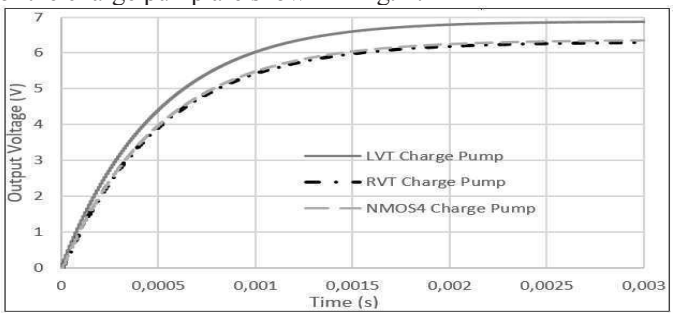

Fig. 4. Output voltage of the charge pump for LVT, RVT and NMOS transistors

As shown in Fig. 4, the charge pump that operated with LVT diode-connected transistors achieved better performances than RVT and NMOS responses. The output voltage is 7 V for LVT charge pump while it was a bit higher than 6 V for RVT and CMOS. In this case, a nearly 16%-output voltage improvement was scored by LVT response compared to CMOS because of the low voltage threshold of its transistors. In addition, it is important to mention that default dimensions of LVT are smaller than NMOS, typically a hundred nanometers compared to a dozen of micrometers.

To go further, a 4-stages Dickson circuit has been simulated using optimal parametric values with FDSOI LVT. The pump performs up to 3V-output voltage from a 250mV-input with no load, and an optimized circuit gives an output of 600 mV at 160 µA. This last result was compared to literature in Table I.

TABLE I. COMPARISON OF LOW-VOLTAGE CHARGE PUMP WORK.

Work	**[1]**	**[2]**	**[3]**	**This work**
Type of work	Simulation	Simulation	1-Chip Integration	Simulation
Process	Standard CMOS	Standard CMOS	65nm CMOS	28nm FDSOI
Number of stages	4	4	3	4-Dickson based
Input-Voltage	1.2 V	1.5 V	0.18 V	0.25 V
Output-Voltage	3.5 V	6 V	0.5 V	0.6 V
Gain	2.9	4	2.78	2.4
Output-Current	>40 µA	>30 µA	10 µA	160 µA

V. CONCLUSION

This paper presents simulation results that compare FDSOI 28nm and standard CMOS 350nm transistors performances. The FDSOI LVT transistor was particularly pointed out for its best voltage threshold that allow higher output voltages in Low-Voltage RF-DC and DC-DC conversions while reducing the overall dimensions. FDSOI technology is more expensive than CMOS but offers many advantages as a smaller die size and better performances. These comparison results lead to the choice of FDSOI technology for the design of a complete integrated rectifying module for RF energy harvesting.

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