A 2.45 GHz ISM Band CPW Rectenna for Low Power Levels

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A 2.45 GHz ISM Band CPW Rectenna for Low Power Levels

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Abstract—This paper presents the design and fabrication of a coplanar waveguide (CPW) rectenna using a sequential modular approach. The rectenna is printed on high permittivity, low-loss board ARLON AD1000 ($\epsilon_r = 10.35$ and $\tan\,\delta = 0.0023$ @ 10 GHz). The rectifier section is realized with a single reverse-biased schottky diode SMS-7630 in reverse topology for which a diode model is obtained at −20 dBm for frequencies $F_0 = 2.45$ GHz and $2F_0 = 4.9$ GHz. The low-pass filter and the impedance matching are synthesized from passive CPW structures. Co-simulation technique is used to overcome CPW simulation limitations and to integrate the diode characteristics. The antenna consists of a circular slot loop antenna with stub matching such that its input impedance is close to 50 Ω. The goal of this work is to design a rectifier to simplify and speed up the fabrication process of a rectenna array. We reduced the number of processes to etch the rectifier on the board and minimized the number of lumped elements. At −20 dBm, simulation of the rectifier with an ideal impedance matching network shows rectification at 2.45 GHz with efficiency of 12.8%. The rectifier and rectenna show efficiency of approximately 10% at an operating frequency of 2.48 GHz.

1. INTRODUCTION

Large scale deployment of high-speed communications networks, both wired and wireless, in modern cities (urban spaces) is key to improve environmental sustainability, economic competitiveness, access to services and lifestyle in a service-oriented economy [1]. To sustain the ever-increasing bandwidth requirements, wired connections shift from copper lines to optical fibres. Concurrently, wireless systems have migrated to a newer generation every ten years. Wireless communications make use of electromagnetic waves of various frequency bands to transfer information between devices. However, only a minute fraction of the electromagnetic energy is intercepted at the receiver: the major part is either dissipated by neighbouring objects in the environment or radiated far away. Energy harvesting or energy scavenging devices can intercept part of this energy to power low energy consumption electronic devices. This task is usually assigned to a converting device known as a rectenna which receives electromagnetic waves and converts it to DC power.

The use of rectennas as a means for electromagnetic energy harvesting has received considerable attention from scientists worldwide, more particularly in the context of smart cities. In those cities, sensor network and IoT devices are ubiquitous. However, the level of electromagnetic emissions in urban environments is strictly regulated. Consequently, rectenna are designed to operate at very low incident electromagnetic power levels to meet the power demands of carefully-designed ultra-low consumption devices, typically consuming a few microwatts of DC power. At such low power operation, rectenna DC conversion efficiency is limited due to losses in the lumped-element components, particularly the schottky diode rectifier element used in rectenna fabrication.

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To overcome this issue, two solutions have been proposed. The first one uses an antenna array to collect more RF power, thus enabling better diode rectifier efficiency. The antenna array solution can become challenging to design, due to the variety of frequency bands in usage in a typical urban environment [2]. The designer has to address multiple issues like crosstalk, broadband or multi-band matching and phase-shifting between the individual antennas. The second option is to combine the outputs of a rectenna array in order to generate the required voltage to power the device. Rectenna array solution are less demanding in terms of design methodology, but they require the realization of several rectenna with highly repeatable characteristics. In the literature, microstrip technology is frequently used to fabricate rectenna [3–5] where vias through the substrate are used to create a connection to the ground plane. This step is difficult to reproduce and increases the time required to build a rectenna array; the introduction of each via implying at least one drilling, through-hole plating and soldering step.

In this work, we propose to use coplanar waveguide (CPW) technology depicted in Figure 1 to construct a rectenna operating in the ISM band 2.4–2.5 GHz. In this technology, the ground planes and the conductive lines are on the same spatial plane. To implement the rectifier section in CPW technology, we start by modelling the response of the Schottky diode under incident microwave excitation at the centre frequency of 2.45 GHz. Then, we design a low-pass filter to smooth the DC output signal by suppressing the first and second order harmonics. Thirdly, we build a narrow-band impedance matching network. Lastly, we build a compact circular slot loop antenna having 50 Ω input impedance to complete the fabrication of the CPW rectenna. The efficiency of the standalone rectifier and the complete rectenna are then studied.

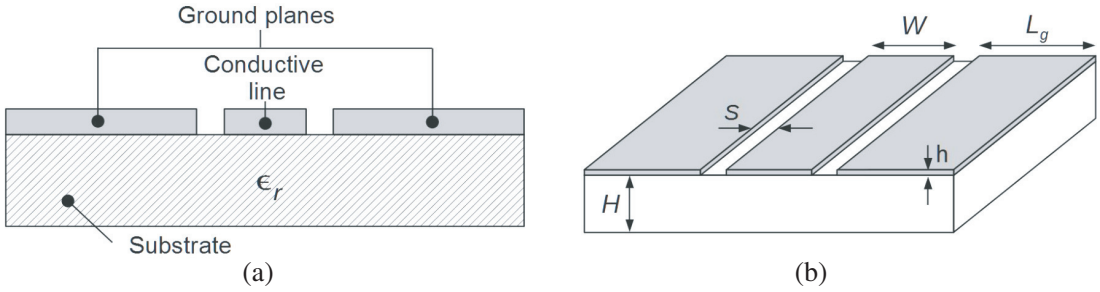


Figure 1. (a) Transversal cut of CPW. (b) Isometric view of CPW.

2. DESIGN REQUIREMENTS AND SUBSTRATE CHOICE

In CPW lines, the electromagnetic fields are concentrated near the copper layer surface in contrast to the well-known microstrip technology where they lie mostly within the dielectric region between the ground plane and the tracks. Several propagation modes can co-exist in CPW lines. The two major propagation modes are called the CPW mode and the coupled-slotline mode. The coupled-slotline mode is not desirable because it is non-TEM and may be excited in presence of discontinuities in circuits such as at Tee-junctions and at parallel stubs. To restrict its propagation, one has to keep the two ground planes balanced and limit track length. In CPW design with discontinuities, air bridges or wire-bonding are used to suppress the unwanted mode. Those structures can be compared to vias in microstrip technology. Firstly, they make fabrication of rectennas more complex and have an adverse effect on its RF performance. Secondly, they have to be precisely placed and soldered when replicating the rectenna, in order to ensure repeatability. In our design, we keep the rectenna circuit symmetric, avoid discontinuities and fabricate the PCB using milling tools only. While CPW rectenna have been proposed previously [4, 6–8], these designs are optimized for high incident power levels and/or use a secondary energy source. In this work, we seek to fabricate a rectenna in CPW dedicated to operation at low power levels near 2.45 GHz and designed towards rectenna array implementation such as in [9].

The choice of the substrate permittivity is dictated by the need for low conductor losses and field containment. With the symbols as defined in Figure 1(b), the effective dielectric constant and the

characteristic impedance are given by:

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k_0')}{K(k_0)} \tag{1}$$

where K is the elliptical integral of the first kind, $k_0 = \frac{W}{W+2S}$ and $k_0' = \sqrt{1-k_0^2}$.

We fabricate the rectenna on an Arlon AD1000 board, which has $\epsilon_r = 10.35$ and $H = 0.762\,\text{mm}$. The CPW lines are designed with slots width $S = 0.787\,\text{mm}$, which is accurately and easily etched by single pass milling with a standard 0.787 mm milling tool bit. A characteristic impedance close to $50\,\Omega$ is achieved with a central conductor width $W = 3.54\,\text{mm}$. The widths of all ground planes are set to $L_g = 20\,\text{mm}$ to ensure proper mode excitation.

3. DIODE MODEL

The Schottky diode SMS7630-001LF [10] is selected for the rectifier section due to its low biasing voltage requirement for a weak input signal. We use a two-step approach to predict the behaviour of the diode when mounted on an Arlon AD1000 CPW line. Initially, we model its DC characteristic under reverse-bias because the rectifier exploits a single series diode in reverse topology. This minimizes loss and the lumped-element component count, while ensuring positive DC output. Secondly, we model the small signal diode behaviour from 2 GHz to 6 GHz at an input signal level of $-20\,\text{dBm}$ for DC bias points from 0 to $-500\,\text{mV}$.

3.1. DC Behaviour

The experimental reverse-bias characteristic of the rectifier was obtained using a Multimeter HP E34401A with a precision of $10\,\mu\text{A}$. The diode DC behaviour was represented by a voltage-controlled current generator. The generator is driven by a polynomial equation optimised through Scilab algorithm to minimize the error between the model current and the measured one in the range 0 to $-2\,\text{V}$. A ninth order Equation (2) was used to represent the current I_{diode} as a function of voltage V. The equation order was chosen through a LMS algorithm. This algorithm select the order equation giving the minimum square error among several equations from order 2 to 12. Figure 2(a) shows comparison of simulated and measured I_{diode} from $-2\,\text{V}$ to $0\,\text{V}$.

$$I_{diode}(V) = 10^3(0.212V + 1.44V^2 + 5.1V^3 + 10V^4 + 11.8V^5 + 8.45V^6 + 3.62V^7 + 0.85V^8 + 0.084V^9)A \tag{2}$$

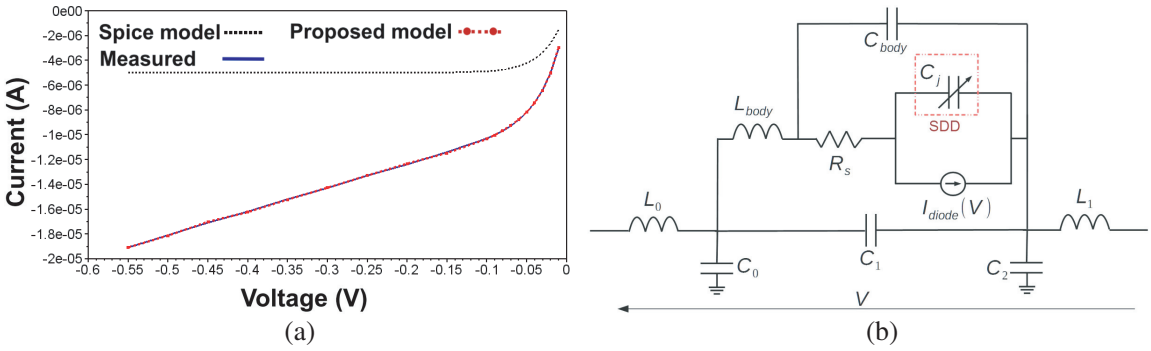


Figure 2. (a) Comparison of DC diode behaviour between measurement, the SPICE model and the proposed model. (b) Diode model.

3.2. RF Behaviour

To model the RF characteristics of the diode, we measure its S-parameters at $-20\,\text{dBm}$ from 2 GHz to 6 GHz. The goal of this modelling step is to predict the RF behaviour of the diode at $F_0 = 2.45\,\text{GHz}$ and

$2F_0 = 4.9\,\text{GHz}$. The diode S-parameters are measured after a CPW TRL calibration with a homemade calibration kit [11].

To simplify the optimization, first we only investigate its behaviour at F_0 with the average DC bias $DC_b = -0.19\,\text{mV}$ from the DC biasing range. In the diode model (Figure 2(b)), the gap under the diode body is modelled with 3 capacitors in pi-topology C_0, C_1, C_2. The two inductors L_0 and L_1 represent the lumped CPW line attached to the diode and the diode connector. The diode body parasitic effects are modelled with a series inductor L_{body} and parallel capacitor C_{body}. The elements values in Table 1 are found through fitting of simulated S-parameters and measured ones. To model the diode RF behaviour from 0 to $-500\,\text{mV}$, we changed the model static junction capacitor C_j in Figure 2(b). Instead we use a dynamic one with a symbolically define device (SDD) element. This capacitance value is driven by the voltage V across it, based on Equation (3).

$$C_j = 0.14 * 10^{-12} * \exp(V) \tag{3}$$

Table 1. Component value of the diode model.

Component	L_0	L_1	R_s	C_{j0}	C_{body}	L_{body}	C_0	C_1	C_2
Value	944 fH	1.8 pH	20 Ω	0.14 pF	3.2 fF	1.5 nH	221 fF	262 fF	216 fF

4. LOW-PASS FILTER

Rectenna designs featured in the literature commonly use a parallel lumped-element capacitor to realize low-pass filters or parallel stubs [12–14]. In CPW technology, for reasons discussed earlier, a symmetrical layout, ideally with two capacitors, is desirable. This method is frequently used to realize broadband 50 Ω impedance match in CPW where the effect of parasitic inductance has to be minimized [15]. However, this solution increases the number of lumped-element components, thus complicating the fabrication of the rectenna. We avoid this issue by adopting a planar realization of the filtering function in CPW as described in the next paragraph.

Besides the dc part, the major components of the spectrum of a half-wave rectified waveform are the fundamental and its first higher order harmonic [16]. Therefore, we use a combination of two notch-filters realized from short-end series stubs to reject these frequencies. For the sake of compactness, as illustrated in Figure 4(a), we etch one CPW filter on the central strip of the main CPW while a slotline filter is etched in the ground plane layer according to [17]. The latter can also be viewed as a defected ground structure (DGS). The length of the (longer) slotline stubs is such that it filters the fundamental (frequency F_0) while that of the (shorter) CPW stubs is set for filtering off the first harmonic. This choice will allow for easier folding of the slotline stub design to increase compactness of the filter as part of our future work. Additionally, etching the filter stub in the ground plane offers narrower rejection bandwidth.

Simulations by [18] have shown that stub length has a prominent effect on the centre frequency of the stopband, with slot width affecting only marginally the fractional bandwidth. Consequently,

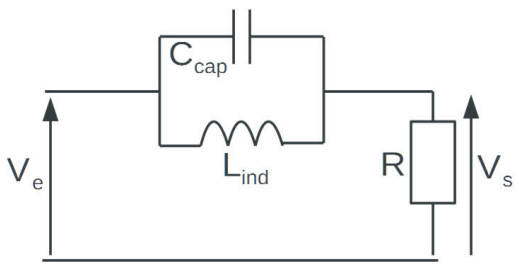
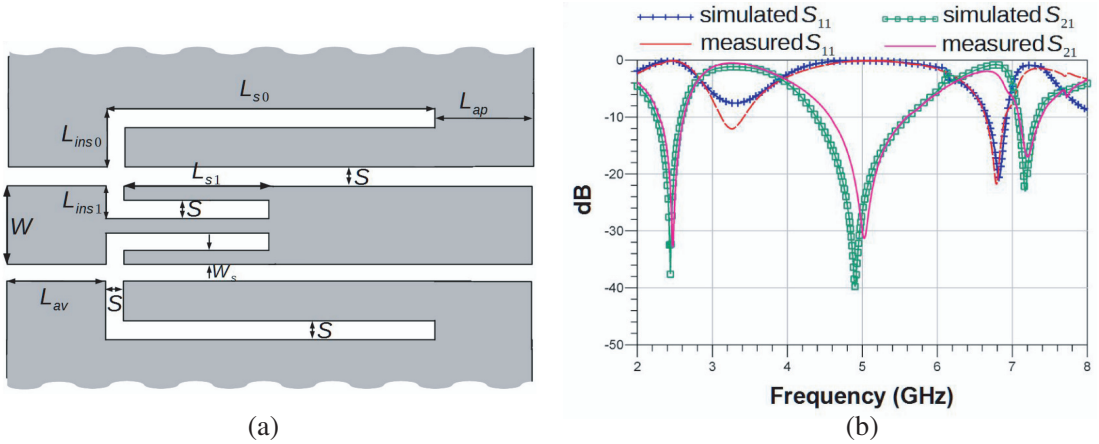


Figure 3. Ideal anti-resonant circuit to represent series short stub in CPW.



(a) (b)

Figure 4. (a) Filter topology. (b) Simulated and measured filter S-parameters. Dimensions of lines are in mm: $L_{s0} = 14.67$; $L_{s1} = 6.7$; $L_{ap} = L_{av} = 5$; $W = 3.64$; $S = 0.787$; $W_s = 0.688$; $L_{ins0} = 3$; $L_{ins1} = 1.476$; $L = 23.5$.

the number of geometrical parameters involved in the filter design is decreased by setting all stub slot widths to the same value of $S = 0.787$ mm as for the main CPW line, while the spacing between the slots etched in the centre conductor are made equal ($Ws = 0.688$ mm) in an effort to maintain symmetry. A method for initial estimation of stub lengths is devised with the assumption that each short-end series stub can be represented by an ideal anti-resonant RLC circuit (Figure 3). This idea is based on the method and analysis conducted in [19]. At frequencies lower than 5 GHz, the stubs are long enough to neglect parasitic effects.

To determine the matrix equation coefficient to predict the length of a stub, two stubs simulations of lengths L_{x0} and L_{x1} are required. For each stub, a pair L_{ind} and C_{cap} are determined with the help of the quality factor Q (4) and the resonant frequency $\omega_0 = \frac{1}{\sqrt{L_{ind}C_{cap}}}$. We chose linear functions to characterise L_{ind} and C_{cap}.

$$Q = \frac{\omega_0}{\omega_{c2} - \omega_{c1}} = \frac{1}{2m} \text{ with } m = \frac{1}{2R}\sqrt{\frac{L_{ind}}{C_{cap}}} \tag{4}$$

Using linear function form $a \cdot L + b$ to characterize L_{ind} and C_{cap} with the stubs length L as the variable, we get the matrix system in Eq. (5) with 4 unknowns and 4 equations.

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} \cdot \begin{bmatrix} L_{x0} & L_{x1} \\ 1 & 1 \end{bmatrix} = \begin{bmatrix} L_{ind0} & L_{ind1} \\ C_{cap0} & C_{cap1} \end{bmatrix} \tag{5}$$

After determination of the coefficients a, b, c, and d values, the resonant frequency of a stub of length L_x can be numerically predicted. With a simple try and error algorithm, the length L_x is sweep until it reaches the desired resonant frequency. This allows fast prediction of a stub length and avoid use of numerous simulation under momentum environment. Due to the hypothesis and simplification to determine the length stub, this method only gives information of the resonant frequency of the stub. In this manner, both stubs have been studied separately and combined afterwards. The resonant frequencies of the stubs are added but a frequency shift appear for L_{s0}. A 1 mm reduction was sufficient on L_{s0} to correct this shift. Figure 4(b) shows the simulated and measured results of the realized filter. As can be seen, it effectively attenuates the signal at F_0 and its first higher order harmonics F_1. In addition to this, the combination of the two stubs enabled the attenuation of the second harmonic $F_2 = 7.35$ GHz.

5. IMPEDANCE MATCHING

5.1. Design and Simulation

An impedance matching network is needed to obtain proper signal transmission from the receiving antenna section to the rectifier section of the rectenna. Additionally bandpass filtering is desirable in order to attenuate out-of-band frequencies that might be received at the antenna. We can combine those two functions in a single design by opting for a narrow bandwidth matching network with centre frequency at $F_0 = 2.45\,\text{GHz}$. This results in overall size reduction of the rectenna. The antenna design is described in the next section, but at this point, it is sufficient to note that it has an impedance of $50\,\Omega$ at the operating frequency. A simulation with an ideal impedance matching network is performed to extract the input impedance that provides the maximum power transfer. The maximum efficiency theo = 12.8% is provided with a resistive load $R_{loadsim} = 5.7\,\text{k}\Omega$.

An L-matching network which does not require air-bridges or wire-bonds is designed to match the $50\,\Omega$ source to the measured impedance $Z_{1m} = 2.8 - j127\,\Omega$ as illustrated in Figure 5(a). This topology (Figure 5(a)) uses a series capacitor and a parallel inductor. The matching circuit elements are implemented as CPW planar structures: a series open stub in the conductive line and a shunt inductance. Initially, each element was designed and optimized separately. Eventually, they were integrated as a compact planar element through a global optimization procedure taking into account parasitic effects and interactions between the elements. The final layout of the impedance matching network, which has $50\,\Omega$ input and output ports is depicted in Figure 5(b). We found it necessary to reduce the width of the series open stub slot S_{mn} from 0.787 mm to 0.508 mm, to improve performance at this stage. The reflection coefficient at the input of the impedance matching network of Figure 5(b) is investigated when its output is connected to a load Z_{1m}. The circuit is numerically simulated under ADS to extract its scattering parameters. The scattering parameters of the impedance matching network are incorporated into an S-parameter block which will be used when modelling the complete rectenna. With the blocks output connected to the optimal load Z_{1m}, the reflection coefficient at the input is simulated. The curve shows a low return loss of $-21\,\text{dBm}$ at the center frequency of 2.45 GHz with a bandwidth of 100 MHz.

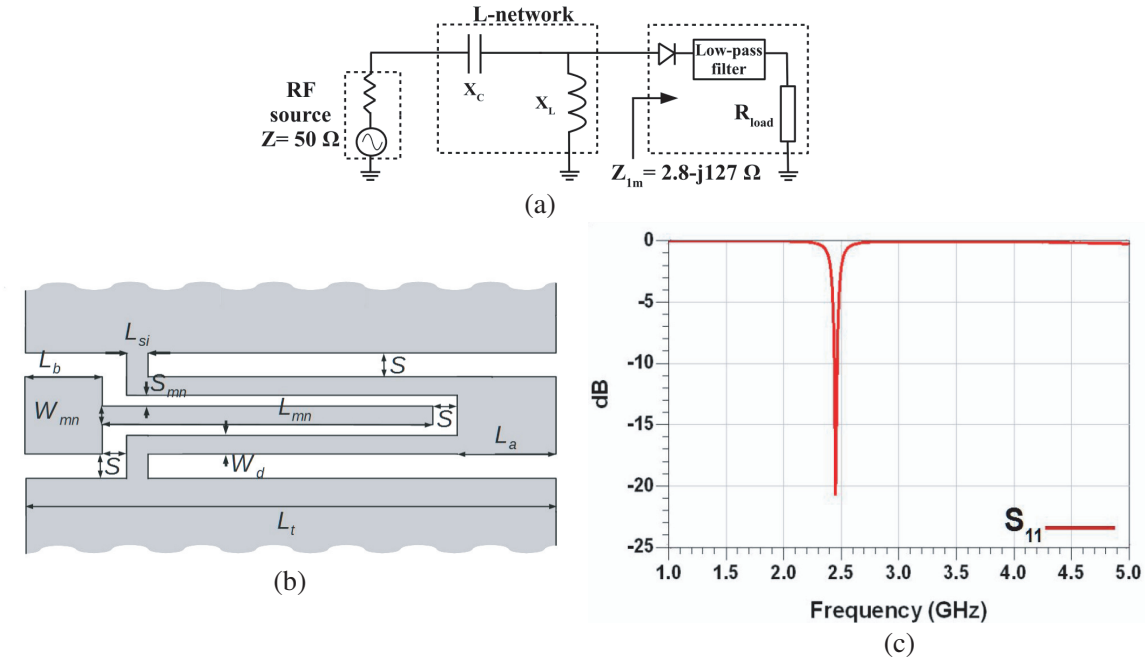


Figure 5. (a) L-network matching circuit. (b) Proposed impedance matching circuit in CPW. (c) Simulated impedance matching reflection coefficient with load Z_{1m}. Dimensions of lines are in mm: $L_{si} = 0.5$; $W_{mn} = 1.5$; $L_{mn} = 7.1$; $L_a = 2$; $L_b = 3.2$; $S_{mn} = 0.508$; $S = 0.787$; $L_t = 12.8$.

5.2. Matching Results

A first realization of the physical device shows a drift in frequency of operation of 55 MHz. We correct this frequency shift, by lengthening the series open stub of the impedance matching circuit by 0.23 mm. The offset simulated matching network was design to match the same load at 2.395 GHz. Measurements carried out on the physical device are represented in Figure 6. Comparison of the measurement and simulation results shows excellent agreement, with the same frequency drift of 55 MHz which lead to proper matching at the desired frequency of 2.45 GHz. But, the reflection coefficient $S_{11} = -9.5$ dB which equals to 88.8% of signal power transmitted.

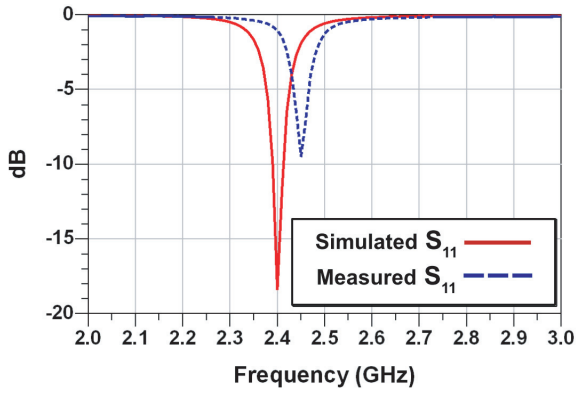


Figure 6. Simulation and measurement comparison of the matching network reflection coefficient.

6. RECTIFIER MEASUREMENTS

The measurement setup of Figure 7(a) is used to evaluate the rectifier performance. An RF generator [20] is used to provide variable incident power from -30 dBm to 0 dBm to the input terminal of the rectifier. The power was calibrated first with a powermeter to take into account the loss in the transmission canal. A numerical multimeter with a precision of 0.0035% measured the voltage. The load and frequency was varied to find the optimum efficiency at -20 dBm. The optimum load value R_{Lm} is equal to the simulated one found in Section 5.1. The measured efficiency is plotted in Figure 7(b) at $F = 2.49$ GHz with efficiency of 9%. The maximum efficiency of 15% is achieved at -9 dBm. When sweeping frequency, it can be noted that the maximum efficiency is achieves at -8 dBm at 2.5 GHz for the same load. We believe that this frequency shift is caused by the narrow bandwidth of the impedance matching network. With the increasing power, the impedance to match shift and the impedance matching network does not act properly. The frequency shifting between measurement in Section 5.2 and measurement of the complete rectifier can be explained by two parameters. Firstly the simulation under ADS does not take into account the coupling effect between the matching network, the diode and low-pass filter in

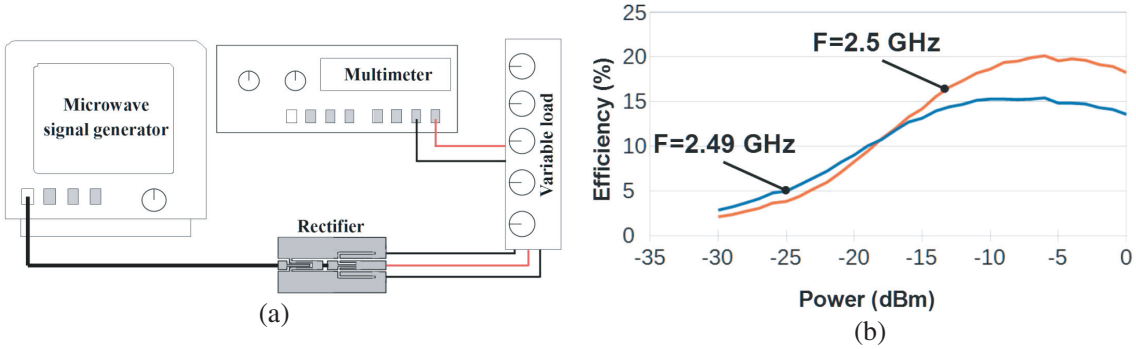
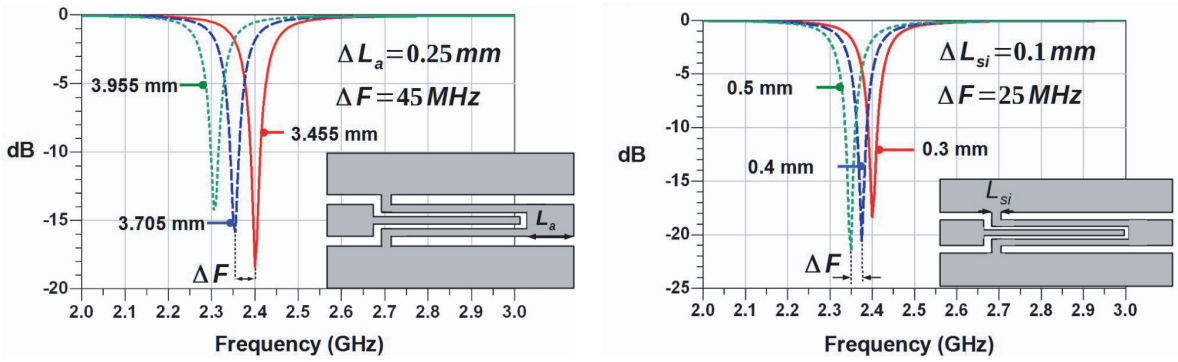


Figure 7. (a) Measurement bench of the rectifier. (b) Measurements comparison of rectifier.



(a) (b)

Figure 8. Sensitivity of the matching network on parameter (a) L_a, (b) L_{si}.

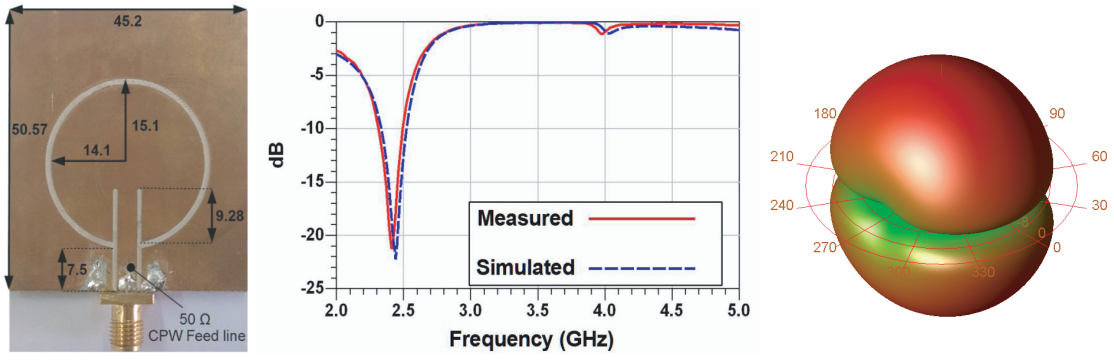
practice. Secondly, the high sensitivity of the matching network over its dimensions. As can be seen on Figure 8(a) and Figure 8(b) for 2 parameters. Drift of 100 µm of L_{si} and 250 µm of L_a lead respectively to frequency shift of 25 MHz and 45 MHz.

To achieve better efficiency at low power levels, as in Section 5.1, we further reduced the slot width S_{mn} to 0.2 mm. This successfully increases the measured efficiency to 10.1% at −20 dBm. This modification also shifted the frequency of operation to 2.48 GHz as can be seen on the next part.

7. CPW RECTENNA MEASUREMENTS

7.1. Antenna Design

A linearly-polarized CPW-fed circular slot loop antenna [21] with input impedance 50 Ω was designed and built to receive electromagnetic waves. Initially, a classical CPW-fed planar circular disc monopole antenna of radius $R = 14.6$ mm, behaving essentially like a leaky resonant cavity, was designed for operation at 2.45 GHz on the AD1000 substrate. The antenna radiation pattern and gain were enhanced by extending the ground plane around the disc forming a slot of width 1 mm. This resulted in a modification of the centre frequency as well as the antenna impedance. The frequency shift was offset by reducing the radius of the disc to $R_0 = 14.1$ mm whereas the antenna impedance was brought to 50 Ω using an inset stub. The antenna was fabricated and fitted with an SMA connector as pictured in Figure 9(a). Numerical simulations results, confirmed by measurements, show that the antenna has a centre frequency of 2.45 GHz, bandwidth of 150 MHz and a gain of 2.3 dBi. Figure 9(b) displays the measured and simulated return losses of the antenna as a function of frequency.



(a) (b) (c)

Figure 9. (a) Photography of the CPW antenna with dimensions in mm. (b) Comparison of measured and simulated reflection coefficient of the antenna. (c) Radiation pattern of the antenna at 2.45 GHz.

7.2. Rectenna Results

The proposed rectenna (Figure 10(a)) have been realized and measured with $S_{mn} = 0.2$ mm to achieve better efficiency. A measurement configuration is adopted whereby a transmitting antenna, fed by a microwave generator, is positioned at a distance of 1.45 m in front of a receiving device. This ensures that the receiver is in the far-field region and that parasitic signals from laboratory equipment are negligible. Measurements are performed at the frequency of 2.48 GHz where maximum rectenna efficiency was recorded. This is close but not identical to the optimum of 2.45 GHz provided by simulation. Initially, a replica of the antenna of Figure 9(a) is placed at the receiver location to record a calibration curve of the received power (by an RF power meter) versus the power setting of the generator. The generator power level is varied such that the calibration curve covered the range from −30 dBm to 0 dBm. During a second phase, the rectenna of Figure 9(a) is placed at the receiver location and the DC power in the 5.7 kΩ load is recorded for various power settings of the microwave generator. These measurements, together with the calibration curve, enable easy computation of the MW to DC efficiency of the rectenna for various power levels collected. Figure 10(b) shows the measured and the simulated efficiency of the rectenna at low received MW power levels. For this purpose the full rectenna have been simulated with the scattering parameters of each rectifier elements and show efficiency of 10.1% at −20 dBm. The measured rectenna efficiency is 9.3%, in excellent agreement with the simulation at −20 dBm. This efficiency rises with increasing power level, reaching a maximum of 16.5% at −10 dBm. The difference between simulation and measurement increases at the same time. This is because the linearised diode model used is valid around −20 dBm incident power: at higher incident power levels, the model is less accurate and impedance match from antenna to load worsens.

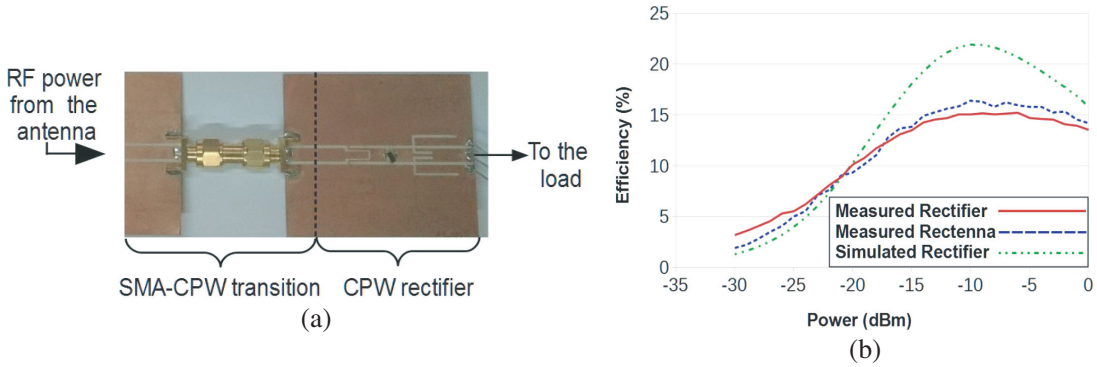


Figure 10. Sensitivity of the matching network on parameter (a) L_a, (b) L_{si}.

8. CONCLUSION

In this work, a simple and easy to fabricate rectenna is realized in CPW with only one lumped element, namely a rectifier diode. The antenna, impedance matching and rectifier sections are investigated separately using numerical simulation and confirmed by measurements. When moving from simulation to practical realization, small shifts in the operating frequency and performance of the rectenna as well as its constitutive elements were observed. Rectifier and rectenna efficiency are respectively measured as 10.1% and 9.3% at 2.48 GHz under a received power of −20 dBm. In order to achieve a better match between simulation and experiment, the use of a full-wave electromagnetic analysis and the availability of more accurate permittivity values of the substrate are essential.

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